

A BPSK demodulator for a crystal-free mote-on-chip

July 20, 2022

Contents

- 1 Introduction
- 2 BPSK; IEEE 802.15.4
- 3 Ideas for BPSK demodulation

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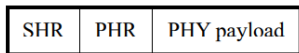
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- SC_μM exclusively uses on-chip oscillators, including a 2.4-GHz LC oscillator to synthesize the communication frequency.
 - LC oscillator drifts at 2100 ppm over a temperature range of 45C.
 - Continuous Calibration (CoCa) : SC_μM tracks and compensates for the drift of its oscillators.
 - BPSK modulation requires efficient phase/frequency synchronization algorithms
- ⇒ How to demodulate the BPSK-modulated IEEE 802.15.4 frames?

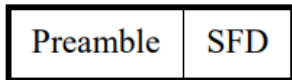
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- The PHY Protocol Data Unit (PPDU) is formatted as:



- The SHR field is formatted as:



- The SFD is a field indicating the end of the SHR and the start of the packet data:

Bits: 0	1	2	3	4	5	6	7
1	1	1	0	0	1	0	1

- The PHR is formatted as:

Bits: 0–6	7
Frame Length	Reserved

- Enhanced Beacon frame format:

Octets: 2	0/1	variable	variable	variable		variable	2/4
Frame Control	Sequence Number	Addressing fields	Auxiliary Security Header	IEs		Beacon Payload	FCS
				Header IEs	Payload IEs		
MHR					MAC Payload		MFR

- BPSK reference modulator block diagram:



- Differential encoding:

$$E_n = R_n \oplus E_{n-1}$$

where

R_n is the raw data bit being encoded

E_n is the corresponding differentially encoded bit

E_{n-1} is the previous differentially encoded bit

- Bit-to-chip mapping:

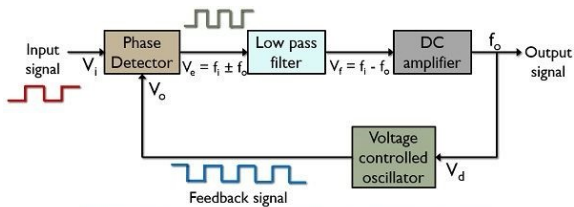
Input bits	Chip values ($c_0 c_1 \dots c_{14}$)
0	1 1 1 1 0 1 0 1 1 1 0 0 1 0 0 0
1	0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 1

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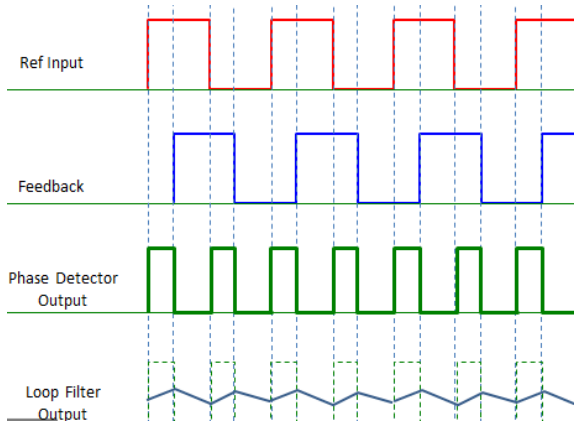
- Step 1: Optical Calibration
 - ⇒ The resulting calibration of the 2-MHz RC oscillator is within the 1000 ppm target
 - ⇒ The calibration of the 2.4-GHz LC oscillator is, however, not within the 40-ppm target
 - Step 2: Frequency Sweep
 - With CoCA, SC_μM sweeps LC frequency setting from (23.31.31) to (24.31.31), listening for Beacon frames
 - SC_μM records the best setting on which it received Beacon frames as its RX frequency setting.
- ⇒ How to correctly receive beacons sent with BPSK modulation?

XOR based PLL

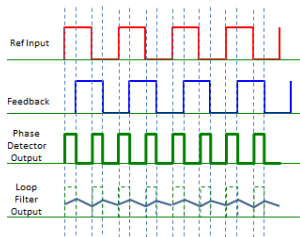
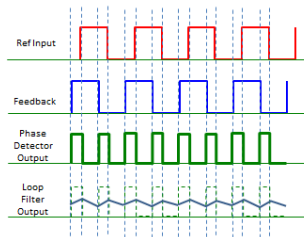


Block Diagram of Phase-Locked Loop

XOR based PLL

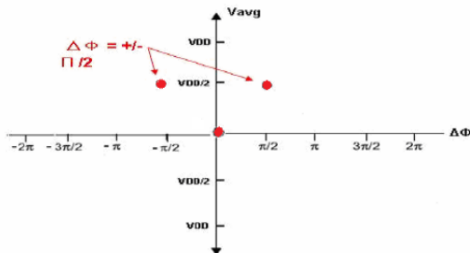


XOR based PLL

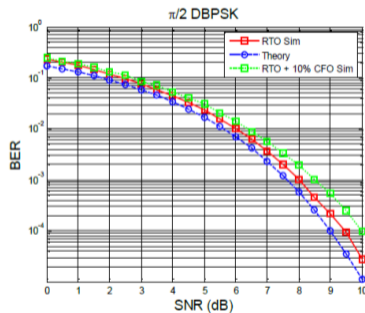
Feedback signal phase is **leading**Feedback signal phase is **lagging**

No difference in Phase
Detector Output and Loop
Filter Output depending on
Leading and Lagging phase

XOR based PLL



- * Frame synchronization
- * Frequency synchronization
- * Time synchronization
- * Phase synchronization



T. Arbi, B. Geller, "Multi-standard Receiver for Medical IoT Sensor Networks," *Chap. 5 Challenges of the Internet of Things, 2018*, Wiley, ISBN : 9781786303615, Sept. 2018.

Thank!