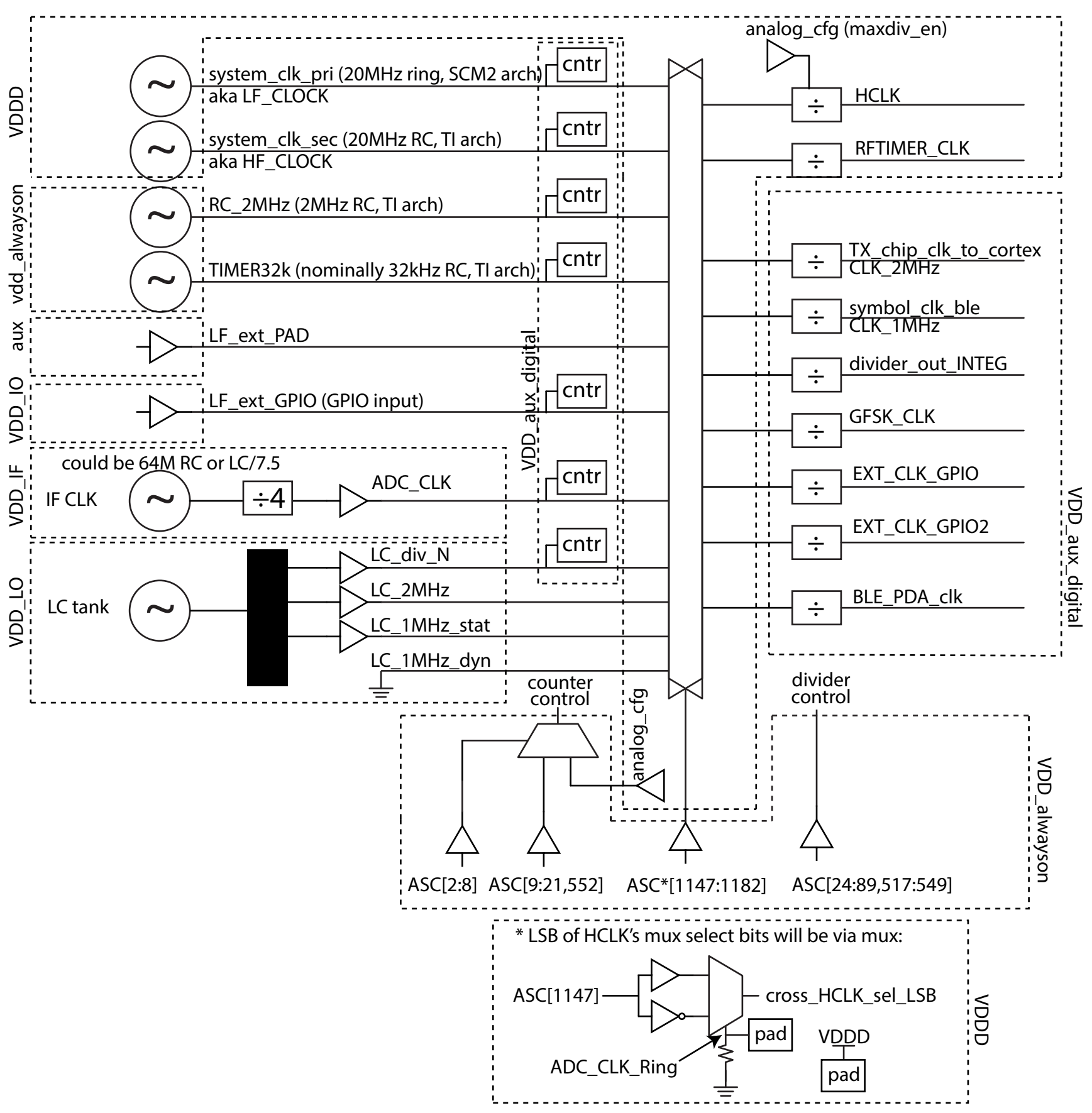
analog_cfg (maxdiv_en)
VDDD
system_clk_pri (20MHz ring, SCM2 arch)
aka LF_CLOCK
system_clk_sec (20MHz RC, TI arch)
aka HF_CLOCK
cntr
HCLK
RFTIMER_CLK
vdd_alwayson
RC_2MHz (2MHz RC, TI arch)
TIMER32k (nominally 32kHz RC, TI arch)
TX_chip_clk_to_cortex
CLK_2MHz
symbol_clk_ble
CLK_1MHz
aux
LF_ext_PAD
divider_out_INTEG
VDD_IO
LF_ext_GPIO (GPIO input)
GFSK_CLK
VDD_aux_digital
VDD_IF
could be 64M RC or LC/7.5
IF CLK
÷4
ADC_CLK
EXT_CLK_GPIO
EXT_CLK_GPIO2
VDD_LO
LC tank
LC_div_N
LC_2MHz
LC_1MHz_stat
LC_1MHz_dyn
BLE_PDA_clk
counter
control
divider
control
analog_cfg
VDD_alwayson
ASC[2:8]
ASC[9:21,552]
ASC*[1147:1182]
ASC[24:89,517:549]
* LSB of HCLK's mux select bits will be via mux:
ASC[1147]
cross_HCLK_sel_LSB
pad
VDDD
ADC_CLK_Ring
VDDD
pad