CMOS oscillators to satisfy 802.15.4 and Bluetooth LE PHY specifications without a crystal reference

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***Abstract*—We compare measured CMOS relaxation oscillator performance against physical-layer specifications defined by low-power RF communication standards IEEE 802.15.4 and Bluetooth Low-Energy with the aim of satisfying those specifications without a crystal oscillator. The time and frequency aspects of these FSK-based specifications concern RF channel, modulation frequency, data rate, and sleep time. If they can be satisfied without a crystal oscillator, future wireless ICs can be designed that do not rely on a crystal reference and still perform standards-compatible communication. We find most physical-layer specifications can be satisfied by relaxation oscillators with the exception of RF carrier accuracy. The RF ring oscillator under test is dominated by flicker noise, which sets an Allan variance/jitter floor about an order of magnitude noisier than is required by current specifications.**

***Keywords*—Crystal-free, crystalless, ring oscillators, RC oscillators, smart dust, Internet of Things.**

I. Introduction

Communication systems based on frequency shift keying (FSK), like IEEE 802.15.4 O-QPSK/MSK PHY [1] or Bluetooth Low-Energy [2], have physical layers defined by four senses of time. The published specification defines accuracy requirements, error bounds, and how to map information to these senses of time.

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These four senses of time are illustrated in Fig. 1: channel frequency, modulation frequency, data rate, and timer. Most of these values have some mean μ and standard deviation (jitter) σ. The exceptions are:

- Modulation frequency, which can lack σ if it is, for instance, controlled by fixed capacitors with no significant time-dependent random error. In our implementation, this quantity is not derived from an oscillator and so is not affected by using CMOS frequency sources instead of a crystal reference. We will ignore it for the remainder of this paper.
- Timer, which has μ but we don't care because its average duration is adjustable dependent on schedule. Timer σ is the important quantity because that determines receiver guard time, which determines average system energy.

The μ and σ specified for 802.15.4 and BLE are compiled in Table I to the extent possible. Some values are specified in absolute terms (Hz) but we have converted them to ppm for consistency. Some specification documents only define aggregate error, such as with data rate, or don't define timer jitter, such as with 802.15.4. In that case, we assume a jitter target to obtain 1.3ms guard time as described in existing published implementations [3].

TABLE I
OSCILLATOR-DERIVED TIME SPECIFICATIONS FOR COMMON LOW-POWER RADIO STANDARDS. ALL VALUES ARE +/-.

Source of time	IEEE 802.15.4 [1] (O-QPSK PHY) mean μ	stddev σ	Bluetooth LE [2] (uncoded PHY) mean μ	stddev σ
Channel	40ppm total $\mu+\sigma$		42ppm	20ppm over packet and 400Hz/us
Data rate	40ppm total $\mu+\sigma$		50ppm total $\mu+\sigma$	
Sleep timer	N/A	30ppm [3]	N/A	500ppm

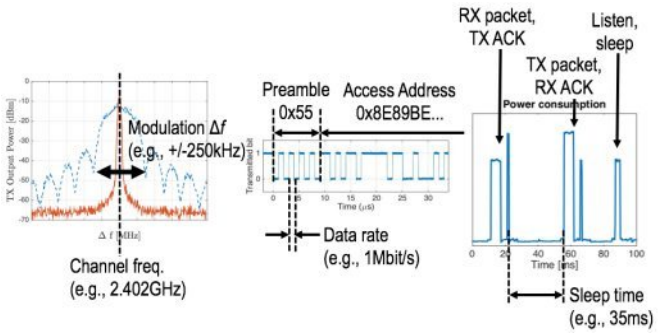

Fig. 1. The four senses of time defining the physical layer of a FSK radio: (a) channel or center frequency (evident in unmodulated red trace) and modulation frequency Δf to define average frequency and denote 1 or 0 by transmitting faster or slower than average (evident in modulated blue trace; null-to-null spacing of modulated waveform is $1.5\Delta f$), (b) data rate ("chip rate" if data is coded, as in 802.15.4, or "bit rate" if uncoded, as in some portions of BLE) to define how often the modulation frequency will change, and (c) sleep timer to define when to wake up and, possibly, communicate.

A. Interpreting BLE carrier drift spec

Taken literally, BLE's carrier drift (accumulated jitter) requirement of $400Hz/\mu s$ is 0.17ppm: two orders more restrictive than a typical crystal. It is unlikely the drift is measured per microsecond but information on the practical evaluation of this specification is sparse. Most test equipment manufacturers state their capability to make BLE carrier drift measurements but lack detail on how the test is performed. For traditional Bluetooth, two manufacturers describe comparing average frequency of adjacent 10-bit sequences, which means a maximum accumulated drift of 4kHz over $10\mu s$ or 1.7ppm [4], [5]. Only one equipment manufacturer describes their BLE-specific tests; they evaluate carrier frequency every $50\mu s$ in the packet payload [6]. The maximum accumulated drift during that test is 20kHz or 8.3ppm, which is closer to a crystal's tolerance. If instead we use the spec defining the maximum frequency drift over an entire $376\mu s$ packet, 50kHz, the resultant 21ppm error tolerance is within typical crystal timing capabilities.

These four ways of interpreting carrier drift are summarized in Table II, marked in Fig. 2 and the least restrictive is marked in Fig. 4. Existing BLE transceiver design literature [7] describes drift requirements as somewhat between our third and fourth interpretation, but lacks a reference for such a conclusion.

TABLE II
FOUR WAYS OF INTERPRETING THE BLUETOOTH LOW-ENERGY CARRIER DRIFT SPECIFICATION

No.	Error	Description
1	$400Hz/\mu s$ (0.17ppm)	As printed in [2]
2	$4kHz/10\mu s$ (1.7ppm)	Adjacent 10-bit sequences
3	$20kHz/50\mu s$ (8.3ppm)	Payload sequences only
4	$50kHz/376\mu s$ (21ppm)	Whole packet

II. COMPARING MEASUREMENTS TO SPECIFICATIONS

The following sections contain measurement results of various CMOS oscillators, the performance of which is compared to wireless specifications a particular oscillator might be used to satisfy. A specification's mean μ is defined by circuit design decisions (predominantly DAC tuning resolution, unless dithering is used) and Allan variance $\sigma_y(\tau)$ plots are used to describe edge uncertainty (jitter, σ) in fractional units after averaging for a particular amount of time. Note that, for some oscillators, error starts *increasing* at long time scales. The typical instinct to average more samples to get more accuracy is invalid in all oscillators after enough time, when higher-ordered noise contributors start to dominate.

Most Allan variance figures in this paper include multiple overlapping traces. These overlapping data sets were taken to overcome sampling speed and memory size limitations of the Agilent 53230A frequency counter with 6GHz input and OCXO timebase options. Plots were generated in Timelab [8].

All data was taken in an indoor open-air lab benchtop environment (i.e., without a temperature chamber). All oscillators have some sensitivity to temperature – and supply voltage, age, etc. – changes, compensation for which is beyond the scope of this paper.

A. Crystal reference

We start with the highest-performing solution: a 10MHz oven-controlled crystal oscillator (OCXO), a class of oscillators known for sub-ppb accuracy. The Allan deviation for this crystal is plotted in Fig. 2. All the specifications described in Table I are 30ppm or greater with the exception of BLE's carrier drift, and a line in Fig. 2 at 30ppm indicates a crystal will meet or exceed those specs, which is expected.

As for BLE carrier drift, we plot the four ways of interpreting the drift spec as described in Section I-A: 0.17ppm at $1\mu s$ intervals, 1.7ppm at $10\mu s$, 8.3ppm at $50\mu s$, and 21ppm at $376\mu s$ – as stars in Fig. 2. The first and second stars are unlikely ways to interpret the drift spec.

If we assume this crystal is the reference oscillator in a PLL, the RF VCO to which it is locked will have the same noise profile at times longer than the loop bandwidth. Assuming a loop bandwidth of 1/10th of the 10MHz crystal or a $1\mu s$ period, all four stars are at periods equal to or greater than that period. Furthermore, the third and fourth stars are the mostly likely ways to interpret BLE drift spec and lie well above the Allan deviation line. Assuming negligible additional jitter contributions by the phase detector, loop filter, and divider, we

Fig. 2. Modified Allan Deviation for a temperature-compensated crystal oscillator. Line at 30ppm denotes lower limit of most specifications from Table I. Stars indicate four ways of interpreting BLE carrier drift described in Section I-A. The leftmost traces in blue and purple, terminating near 10ms and 100ms respectively, are from frequency measurements every $1\mu s$. Green rightmost trace terminating near 100s is from measurements every 1ms.

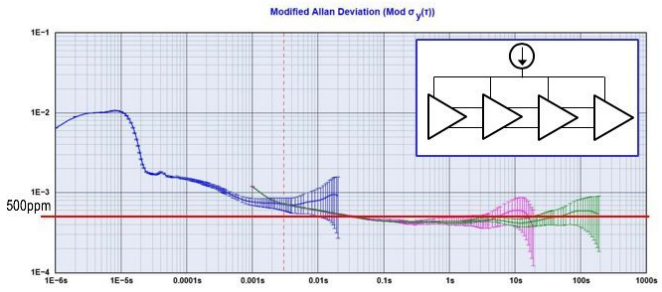

Fig. 3. Modified Allan Deviation for a low-power CPU clock. Line at 500ppm corresponds to the least restrictive timing spec from Table I; clearly, this class of clock is inappropriate for radio timing. The leftmost trace in blue is from frequency measurements every $1\mu s$; the middle and rightmost traces in purple and green, respectively, are from measurements every 1ms.

therefore predict the VCO will meet the RF carrier drift spec and hence a crystal-based RF system passes all specifications, as expected.

B. CPU clock

Ring oscillators are small, low power, and often included in SoCs to provide digital clock sources. We fabricated one such oscillator: a current-starved 4-stage differential ring, with current DAC to adjust speed. It consumes $1.5\mu A$ at 20MHz in extracted simulation. The real current draw is too small to measure against our SoC's baseline. This oscillator's measured Allan deviation is plotted in Fig. 3 with a line at the most relaxed specification: 500ppm for BLE's timer. While this clock is fine for operating a CPU, it is clearly not suitable for RF timing.

C. Free-running RF ring oscillator

Ring oscillators running at RF speeds often serve as the adjustable oscillator in a PLL-based frequency synthesizer. The PLL uses a crystal oscillator as a more pure frequency reference and thereby turns an ordinarily-noisy RF oscillator into something that can meet radio spec. This traditional technique is successfully used in commercial products and, more importantly, depends on an external crystal, so we

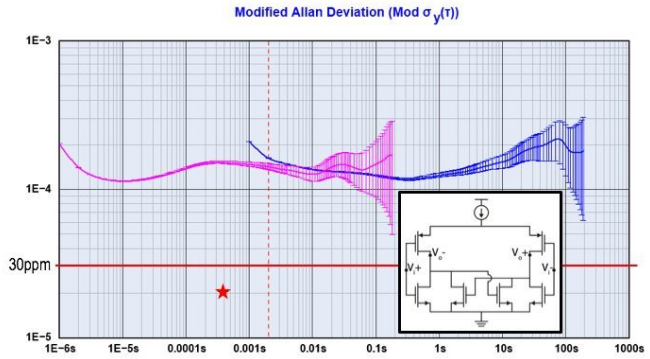

Fig. 4. Modified Allan Deviation for a free-running 2.44GHz ring oscillator. Line at 30ppm denotes lower limit of most specifications from Table I. Star indicates the most relaxed, highest-drift, of the four ways of interpreting BLE carrier drift described in Section I-A: 21ppm at $376\mu s$. Leftmost purple trace is from frequency measurements every $1\mu s$. Rightmost blue trace is from measurements every 1ms. Inset: schematic of individual delay cell; eight are linked together to form oscillator.

consider a free-running RF oscillator in this section. The oscillator under test is an 8-stage differential current-starved ring with kick-start circuit to prevent latching. The schematic for each stage, or delay cell, is shown in the inset of Fig. 4. It consumes 1.25mW and was tuned to 2.44GHz manually prior to measurement.

Measured results are shown in Fig. 4. The results miss most specifications but are close enough to motivate refining future designs. We see flatness across the majority of the plot indicating flicker noise dominates in the range of useful time metrics. The white noise-dominant region likely lies at time scales shorter than $1\mu s$, out of the range of our instruments.

D. Data clock w/ 2MHz RC oscillator

A frequency synthesizer can potentially supply all necessary frequency sources but, by running crystal-free, we don't have that option. Instead, we designed a 2MHz RC oscillator to generate the 802.15.4 data clock directly and BLE data clock via a fixed divide-by-2 block. It was based on the design in [9] but without the flipped replica inverter regulator to reduce complexity. It consumes $2\mu A$, which could be a significant savings compared to deriving this frequency source from a synthesizer. This is particularly useful because the power needed to generate this clock is drawn simultaneously with LO generation and PA power during transmission, thus reducing minimum peak power. Its adjustable resistor DAC was designed to have 27ppm tuning resolution.

Its Allan deviation is plotted is Fig. 5 with markers indicating the oscillator barely exceeds jitter specifications for 802.15.4 ($0.5\mu s$ chip period) and BLE ($1\mu s$ bit period). While jitter alone meets specifications, 27ppm tuning resolution means the starting frequency could be at most ± 13.5ppm off. That initial static error, combined with measured jitter, may exceed 40 or 50ppm and therefore miss specifications. We are confident a simple redesign to increase tuning resolution with a finer resistive DAC, and/or sizing inverters to consume

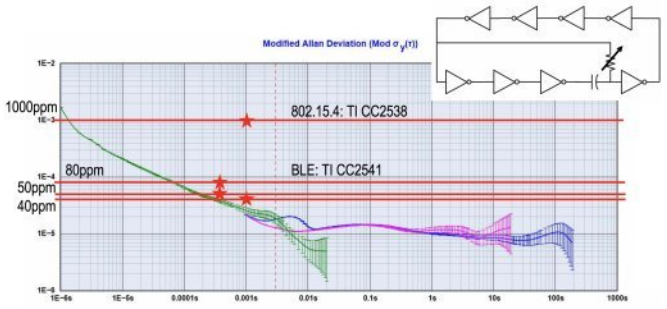

Fig. 5. Modified Allan Deviation for a 2MHz RC oscillator based on [9]. Lines at 40 and 50ppm indicate specifications for 802.15.4 and BLE, respectively, with stars marking their respective chip/bit periods. Lines at 80ppm and 1000ppm indicate actual data sheet requirements for Texas Instruments CC2541 (BLE) and CC2538 (802.15.4), respectively [10], [11], with stars marking corresponding chip/bit periods. Leftmost trace in green is from frequency measurements every $1\mu s$. Purple and blue rightmost traces are from measurements every 1ms.

Fig. 6. Allan Deviation for a 32kHz RC oscillator based on [9]. Lines at 30ppm and 500ppm indicate specifications from Table I. Green and pink traces are from repeated 1000s lab measurements. Red trace is from lab measurement lasting 10000s; over this time period, temperature change in the room is significant enough to manifest as random walk error and causes error to grow after approx. 100s. Blue trace is from 64ms of transient noise simulation showing good, but optimistic, agreement with measurement. Note: Allan Deviation was used instead of Modified Allan Deviation in this plot to better visually identify overlap between 1000s and 10000s measurements.

more power and thereby contribute less jitter, would meet specification.

Practically, however, off-the-shelf parts are more generous than published specifications. Included in Fig. 5 are lines indicated real-world receiver datasheet limits, which this oscillator meets.

E. Sleep timer w/ 32kHz RC oscillator

The 2MHz oscillator in Section II-D would suffice for sleep timing as well, but sleep timer requirements are much more lax than a data clock so we know we have an opportunity to save power. A re-designed oscillator based on [9] was implemented for this purpose, including the additional LDO stage as in the source design, consuming simulated 350nA. The real current draw is again too small to measure against our SoC's baseline. It was targeted for 32kHz operation but lacks any tuning because the true center frequency does not matter; after calibration step to measure its frequency, e.g., receiving two packets with known interstitial time as described in Sec. III of [12], a timer can be set with an appropriate number of ticks to achieve a given sleep time.

The measured jitter of this oscillator is plotted in Fig. 6 with relevant sleep timer specifications indicated. Because of how this timer is used, it makes more sense to plot time deviation: instead of fractional error after a given time (Allan deviation $\sigma_y(\tau)$), we are more interested in absolute error in seconds after a given time (time deviation $\sigma_x(\tau)$). This method of interpreting our results is plotted in Fig. 7. Both specifications target approximately 1ms guard time. In BLE, this goal is mentioned in Section 4.2.2, "Sleep Clock Accuracy," of [2] in describing the "anchor point" for the timing of a packet exchange event. There is no explicit guard time specified in 802.15.4, but in a practical implementation of OpenWSN it is 1.3ms for the packet and 0.5ms for the acknowledgement [3].

The plotted time deviation indicates 1ms jitter will result after waiting for about 105s. Given error bars, and the fact that jitter only describes error magnitude of only 1 standard deviation, a system using this sleep timer would likely be designed to sleep no longer than 20s to ensure reliable communication with a 1ms guard time.

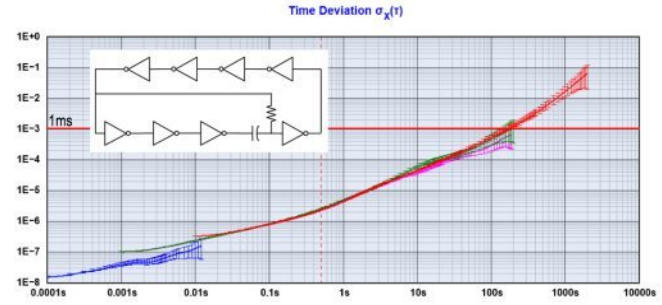

Fig. 7. Time deviation for a 32kHz RC oscillator based on [9]. Line at 1ms indicates reasonable wakeup time error goal, or guard time, for BLE and 802.15.4 specifications. Green and pink traces are from repeated 1000s lab measurements. Red trace is from lab measurement lasting 10000s. Blue trace is from 64ms of transient noise simulation showing good, but optimistic, agreement with measurement.

III. Summary of Results

A summary of specifications, relaxation oscillators designed to meet to them, and whether the given oscillator meets the specification, is given in Table III. Data clock and sleep timer are met, whereas the implemented RF ring oscillator is dominated by flicker noise as indicated by the relative flatness of the Allan deviation. The measured noise floor is and is at least 70ppm beyond the specification goal. Because flicker dominates the behavior of this oscillator, the instinct to spend more power to reduce white noise doesn't apply and may exacerbate observed noise levels via increased flicker noise.

Though the RF oscillator's performance misses the specifications examined in this paper, existing work on communication with free-running ring oscillators indicates relaxing IEEE 802.15.4 modulation frequency specifications from ± 0.5MHz FSK to ± 1MHz FSK would allow 802.15.4-quality communication ($< 1\%$ PER) [13].

TABLE III
SUMMARY OF SPECIFICATION AND OSCILLATOR PERFORMANCE COMPARISONS

Spec type	Oscillator	Specification summary	Meets?
Channel	Ring, Sec. II-C	40ppm $\mu + \sigma$ (802.15.4)	N
		42ppm $\mu+$ Sec. I-A (BLE)	
Data clock	RC, Sec. II-D	40ppm $\mu + \sigma$ (802.15.4)	Y
		50pm $\mu + \sigma$ (BLE)	
Sleep Timer	Sub-Thresh.	1.3ms [3] σ (802.15.4)	Y
	RC, Sec. II-E	1ms σ (BLE)	

IV. 32kHz SLEEP TIMER JITTER CALCULATION AND SIMULATION

The 32kHz timer oscillator is straightforward to analyze by hand, and it is the most computationally tractable to simulate by virtue of its low speed, so we use it to evaluate to what extent theory and measurement agree in this experiment. Jitter was evaluated four different ways, the results of which are compiled in Table IV and described below.

A. Hand calculations

To estimate jitter by hand, we first recognize this oscillator's performance is dominated by the relaxation of the large static R and C passives. A jitter estimate can be performed by comparing voltage noise at the RC node with slew rate at the time of transition. If we assume noise is dominated by the integrated noise on the large 10pF capacitor, $\overline{v_n^2} = kT/C = 4{*}10^{-21}/10{*}10^{-12}$ so $v_n = 20\mu V$. The RC node swings with amplitude $2V_{DD}$ and transitions at approximately $V_{DD}/2$, so we say the RC decay is about 2/3 to its final value before switching or lasts $1\tau = 1/RC$. One RC decay is about $1.5V_{DD}$ so we can say $dv/dt = 1.5 * 1/\tau * V_{DD} * 1/e = 19.7mV/\mu s$. This estimate matches well with simulation. Hence, 1σ of dt uncertainty at the RC is about 1ns, or 36ppm.

Being deep submicron transistors biased in subthreshold, we rely on simulation to estimate gain of an inverter with input at $V_{DD}/2$: about 11V/V. This RC oscillator is effectively a single-ended ring oscillator with a dominant noise source in the middle. We know single-ended ring jitter can be estimated by calculating the jitter of a single stage [14]. Hence, we can conclude expected jitter in this rough approximation to be kT/C noise times gain of one stage: about 11ns or 360ppm.

B. Simulation

We performed a transient noise simulation of this oscillator, along with transistor-level schematics of current and voltage sources supplying it, for 64ms with noise bandwidth 1Hz to 100MHz. Period measurements of results have standard deviation of 14.5ns 464ppm. Period simulations were averaged into 0.1ms groups and plotted alongside measurements in Fig. 6 and Fig. 7. We can again choose a point in the white noise region of the time deviation plot and scale by the square root of the period ratio. Using this method, simulated jitter is estimated to be a more optimistic 7.1ns or 226ppm.

TABLE IV
COMPARISON OF 32kHz OSCILLATOR JITTER DETERMINED THROUGH HAND CALCULATION, SIMULATION, AND MEASUREMENT

Source	Method	Period Jitter (ns)	Period Jitter (ppm)
Calc	Voltage noise on RC node	11	360
Sim	Tran noise stddev	14.5	464
Sim	Time dev. extrapolation	7.1	226
Meas	Time dev. extrapolation	14.1	452

C. Measurement extrapolation

We can estimate real period jitter by extrapolating our time deviation data: starting from a point in the white noise region of the plot in Fig. 7 (e.g., $0.8\mu s$ error at 0.1s period) and scaling by the square root of the period ratio, measurement period jitter is estimated to be 14.1ns or 452ppm. This is somewhat noisier than hand-calculation and about twice as noisy as simulation when comparing results extrapolated from time deviation plots. Simulated and measured data are plotted in Figs. 6 and 7 where the similarities are evident, despite the comparatively low amount of simulated data available.

V. CONCLUSION

We have described timing specifications of the physical layer of two major FSK-based radio standards – IEEE 802.15.4 and Bluetooth Low-Energy – and compared measurements of various CMOS oscillators against aspects of those standards. Our goal was to determine to what extent current radio standards can be satisfied without off-chip crystal references. Sleep timing and data clock requirements can be satisfied with RC oscillators. Frequency shifts to transmit FSK data can be accomplished by, for instance, switching capacitors in and out of the oscillator, which needs no crystal even in a traditional system. RF ring oscillator results miss specifications by about an order of magnitude but we have hope for future designs if flicker noise dominance issues can be avoided. Finally, we presented an example to illustrate the comparison between theory, simulation, and measurement in relaxation oscillators which shows promising simulator results but still underscores the importance of fabrication and measurement before oscillator results can be relied upon.

If RF communication systems can relax their reliance on external reference oscillators, it is possible to design a wireless sensor mote with zero external components resulting drastic reductions in size, power consumption, and cost. These gains can be realized while maintaining advantages of standards-compatible communications like peer-to-peer communications without a high-fidelity base station (as in, e.g., RFID) and interoperation with billions of COTS devices.

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